REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Non-Final Office Action dated February 14, 2008 has been received and its contents carefully reviewed.

Claims 1, 4, 22 and 24 are hereby amended. Accordingly, claims 1-25 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, claims 1-9, 13-14, 16 and 22-25 are rejected under 35 USC 103(a) as being unpatentable over Ishii (U.S. Patent No. 6,670,944) in view of Kim (U.S. Pub. No. 2003/0128180), and futher in view of Kanzaki (U.S. Patent No. 6,967,639).

The rejection of claim 1 is respectfully traversed and reconsideration is requested. Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "a shift register provided with first and second half-period clock signals having phases inverted with respect to each other, first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period, a start pulse, a high-level supply voltage and a low-level supply voltage, wherein the shift register generates a half-period output in response to the start pulse and the first and second half-period clock signals, and generates a one-period output at a half-period delay from an end time of the half-period output in response to any one of the first to fourth one-period clock signals, and wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals." However, none of the cited references including Ishii, Kim and Kanzaki, singly or in combination, teaches or suggests at least this feature of the claimed invention. The clock signals (CLK and CLKinv) of Ishii do not have a pulse width that is half of the pulse width of the first and fourth clock signals (C1 to C4) of Kim. Accordingly, applicant respectfully submits that claims 1 to 3 are allowable over the cited references.

The rejection of claim 4 is respectfully traversed and reconsideration is requested. Claim 4 is allowable over the cited reference in that claim 4 recite a combination of elements including, for example, "a first input circuit for charging a first charge control node in response to a start pulse and a first half-period clock signal of first and second half-period clock signals

having phases inverted with respect to each other and each having a half-period pulse width, and for charging a first discharge control node in response to the first half-period clock signal and a first clock signal of first to third clock signals having phases shifted sequentially and each having a one-period pulse width; and a first output circuit for outputting a half-period output to an output node in response to a control signal from the first charge control node and the second half-period clock signal, and for discharging the output node in response to a control signal from the first discharge control node, wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. The clock signals (CLK and CLKinv) of Ishii do not have a pulse width that is half of the pulse width of the first and fourth clock signals (C1 to C4) of Kim. Accordingly, applicant respectfully submits that claims 4 to 21 are allowable over the cited references.

The rejection of claim 22 is respectfully traversed and reconsideration is requested. Claim 22 is allowable over the cited reference in that claim 22 recite a combination of elements including, for example, "receiving first and second half-period clock signals having phases inverted with respect to each other and each having a half-period of pulse width, first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period, a start pulse, a high-level supply voltage and a low-level supply voltage; and generating a half-period output in response to the start pulse and the first and second half-period clock signals, and generating an one-period output at a half-period delay from the end time of the half-period output in response to any one of the first to fourth one-period clock signals, wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. The clock signals (CLK and CLKinv) of Ishii do not have a pulse width that is half of the pulse width of the first and fourth clock signals (C1 to C4) of Kim. Accordingly, applicant respectfully submits that claim 22 and 23 are allowable over the cited references.

The rejection of claim 24 is respectfully traversed and reconsideration is requested. Claim 24 is allowable over the cited reference in that claim 24 recite a combination of elements including, for example, "charging a first charge control node in response to a start pulse and a

first half-period clock signal of first and second half-period clock signals having phases inverted with respect to each other and each having a half-period pulse width; outputting an half-period output to an output node in response to a control signal from the first charge control node and the first half-period clock signal; charging a first discharge control node in response to the second half-period clock signal and a first clock signal of first to third clock signals having phases shifted sequentially and each having an one-period pulse width; discharging the output node in response to a control signal from the first discharge control node; charging the second charge control node in response to the half-period output and the second half-period clock signal; charging the second discharge control node in response to the second clock signal; outputting a one-period output to the output node at a half-period delay from an end time of the half-period output in response to a control signal from the second charge control node and the third clock signal; and discharging the output node in response to a control signal from the second discharge control node, wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. The clock signals (CLK and CLKinv) of Ishii do not have a pulse width that is half of the pulse width of the first and fourth clock signals (C1 to C4) of Kim. Accordingly, applicant respectfully submits that claims 24 and 25 are allowable over the cited references.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: **8 May 2008**

Respectfully submitted,

By: _____

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